What is claimed is:

1. A semiconductor device comprising:

a substrate;

a semiconductor layer of a first conductivity type having a single-crystal structure;

a plurality of transistors each including a first gate electrode provided above said semiconductor layer with a first gate insulation film laid therebetween, a pair of impurity regions of a second conductivity type being provided in said semiconductor layer and becoming a drain region and a source region, and a channel body of the first conductivity type provided in said semiconductor layer at a portion between these impurity regions;

a first gate line for common connection of the first gate electrodes of said plurality of transistors;

a dielectric layer provided above said substrate in an extension direction of said first gate line, for supporting said semiconductor layer under said pair of impurity regions to thereby dielectrically isolate between said substrate and said semiconductor layer;

a second gate electrode provided above said substrate in such a manner as to underlie the channel bodies of said plurality of transistors and oppose said channel bodies with a second gate insulation film laid therebetween, said second gate electrode having a gate length larger than a onefold value of a gate length of said first gate electrode and yet less than or equal to thrice the gate length; and

a second gate line provided above said substrate along the extension direction of said first gate line while being placed between portions of said dielectric layer underlying said pair of impurity regions, said second gate line being for common connection of a plurality of said second gate electrodes.

2. The device according to claim 1, wherein said first gate line includes a word line and wherein said plurality of transistors include memory transistors each being for

storing data based on a majority carrier accumulation state of said channel body.

3. The device according to claim 2, further comprising:

an isolation portion for insulative isolation between adjacent ones of said memory transistors, said isolation portion having a bottom positioned at a lower level than said semiconductor layer.

4. The device according to claim 2, further comprising:

an isolation portion continuously formed in a direction for intersection with said word line, for dielectrically isolating between adjacent ones of said memory transistors.

5. The device according to claim 2, further comprising:

an isolation portion for insulative isolation between adjacent ones of said memory transistors, wherein said second gate line is connected to said substrate at a location underlying said isolation portion.

6. The device according to claim 5, further comprising:

a plug as connected through said substrate to said second gate line.

7. The device according to claim 2, further comprising:

a plug dielectrically isolated from said substrate and connected to said second gate line.

8. The device according to claim 2, wherein said semiconductor layer is such that a formation region of said channel body is less in thickness than a formation region of said impurity region.

9. The device according to claim 2, wherein a bit line crossing said word line is connected to said drain region, and wherein a source line provided along an extension direction of said word line is connected to said source region.

10. The device according to claim 2, wherein a logic circuit using transistors formed at said semiconductor layer as its constituent elements is mounted together on said substrate.

11. The device according to claim 10, wherein said semiconductor layer is such that a formation region of said logic circuit is greater in thickness than a formation region of each said memory transistor.

12. The device according to claim 2, wherein each of said plurality of memory transistors stores any one of a first data state in which said channel body retains a certain amount of majority carriers and a second data state in which said channel body retains majority carriers less in amount than those in the first data state.

13. The device according to claim 1, further comprising:

a logic transistor arranged by connecting together one of said pair of impurity regions of said plurality of transistors while connecting together remaining ones of the pairs of impurity regions.

14. The device according to claim 13, wherein a plurality of first gate lines each similar to said first gate line and a plurality of second gate lines each similar to said second gate line are provided to have stripe shapes respectively.

15. A semiconductor device comprising:

a substrate;

a semiconductor layer of a first conductivity type having a single-crystal structure;

a plurality of transistors each including a first gate electrode provided above said semiconductor layer with a first gate insulation film laid therebetween, a pair of impurity regions of a second conductivity type being provided in said semiconductor layer and becoming a drain region and a source region, and a channel body of the first conductivity type provided in said semiconductor layer at a

portion between these impurity regions;

a first gate line for common connection of the first gate electrodes of said plurality of transistors;

a dielectric layer provided above said substrate in an extension direction of said first gate line, for supporting said semiconductor layer under said pair of impurity regions to thereby dielectrically isolate between said substrate and said semiconductor layer;

a second gate electrode provided above said substrate in such a manner as to underlie the channel bodies of said plurality of transistors and oppose said channel bodies with a second gate insulation film laid therebetween;

a second gate line provided above said substrate along the extension direction of said first gate line while being placed between portions of said dielectric layer underlying said pair of impurity regions, said second gate line being for common connection of a plurality of said second gate electrodes; and

an isolation portion for insulative isolation between adjacent ones of said transistors, said isolation portion having a bottom positioned at a lower level than said semiconductor layer.

16. A semiconductor device comprising:

a substrate;

a semiconductor layer of a first conductivity type having a single-crystal structure;

a plurality of transistors each including a first gate electrode provided above said semiconductor layer with a first gate insulation film laid therebetween, a pair of impurity regions of a second conductivity type being provided in said semiconductor layer and becoming a drain region and a source region, and a channel body of the first conductivity type provided in said semiconductor layer at a portion between these impurity regions;

a first gate line for common connection of the first gate electrodes of said plurality of transistors;

a dielectric layer provided above said substrate in an extension direction of said first gate line, for supporting said semiconductor layer under said pair of impurity regions to thereby dielectrically isolate between said substrate and said semiconductor layer;

a second gate electrode provided above said substrate in such a manner as to underlie the channel bodies of said plurality of transistors and oppose said channel bodies with a second gate insulation film laid therebetween; and

a second gate line provided above said substrate along the extension direction of said first gate line while being placed between portions of said dielectric layer underlying said pair of impurity regions, said second gate line being for common connection of a plurality of said second gate electrodes,

wherein said semiconductor layer is such that a formation region of said channel body is less in thickness than a formation region of said impurity region.

17. A method for fabricating a semiconductor device with a plurality of transistors each including a semiconductor layer of a first conductivity type having a single-crystal structure and being dielectrically isolated by a dielectric layer from a substrate, a first gate electrode provided over this semiconductor layer through a first gate insulation film, a pair of impurity regions of a second conductivity type provided in said semiconductor layer for use as a drain region and a source region, and a channel body of the first conductivity type as provided in said semiconductor layer at a location between these impurity regions, said method comprising:

forming an etching stopper having an opening at a crossing portion of a first gate line formation region in which a first gate line is formed for common connection of said first gate electrode and an isolating portion formation region in which an isolating portion is formed for insulative isolation of said plurality of transistors;

etching said dielectric layer with said etching stopper being formed in such a manner that part of said dielectric layer remains under said semiconductor layer in which said pair of impurity regions are to be formed and remains along an extension direction of said first gate line formation region to thereby form an etching region having a cavity at a location beneath a portion of said semiconductor layer whereat said channel body is to be formed along an extension direction of said first gate line formation region;

forming a second gate insulation film in contact with a portion of said semiconductor layer exposed at said cavity;

forming a second gate line for common connection of said second gate electrodes in said etching region along the extension direction of said first gate line formation region in such a manner that a second gate electrode is provided through said second gate insulation film; and

forming in said first gate line formation region said first gate line for common connection of said first gate electrodes in such a manner that said first gate electrode is positioned via said first gate insulation film over said semiconductor layer in which said channel body is formed.

18. The method according to claim 17, further comprising, between the step of forming said etching region and the step of forming said second gate insulation film:

thinning by etching the portion of said semiconductor layer which is exposed at said cavity and which becomes said channel body.

19. The method according to claim 17, wherein the step of forming said etching stopper includes:

forming a lower layer portion of said etching stopper in such a manner as to cover said semiconductor layer;

selectively removing said semiconductor layer and said lower layer portion positioned in said isolating portion formation region;

forming, after the selective removal step, an upper layer portion of said etching stopper so as to cover said

lower layer portion and said dielectric layer; and

selectively removing said upper layer portion being placed in said first gate line formation region.

20. The method according to claim 19, wherein the step of forming said second gate line includes:

forming by vapor phase growth a conductive film in said etching region; and

patterning said second gate line by etching said conductive film with said lower layer portion of said etching stopper being left between neighboring isolating portion formation regions to thereby thin said conductive film of said isolating portion formation region.